Paper No. 14

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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Ex parte JOSE L. MUNOZ and W. ROBERT BERNECKY

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Appeal No. 1998-2093
Application No. 08/303,809

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ON BRIEF

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Before THOMAS, FLEMING, and BLANKENSHIP, Administrative Patent Judges.

BLANKENSHIP, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the examiner's final rejection of claims 1, 4-8, 12, 13, 16, 17, and 19, which are all the claims remaining in the application.

We reverse.

BACKGROUND

The invention is directed to a process for using a shared memory for transferring data between computers in a multi-processor system. Representative claim 1 is reproduced below.

> 1. A process for improving the transfer of data between computers in a multi-processor system via a shared memory, comprising the steps of:
>
> providing a provider computer and a consumer computer, each having a local memory and each linked to said shared memory;
>
> selecting data stored in the local memory of said provider computer for transfer from the local memory of said provider computer to the shared memory;
>
> mapping a portion of said shared memory having a known address for the storage of said data;
>
> communicating the address of the mapped portion to said consumer computer prior to transferring said data;
>
> transmitting a first signal to said provider computer that said consumer computer is ready to receive and extract data from said shared memory;
>
> transferring said selected data from said local memory of said provider computer to said known address in said shared memory after said provider computer receives said first signal;
>
> transmitting a second signal from said provider computer to said consumer computer that said selected data is available in said mapped portion for extraction by said consumer computer;
>
> accessing said selected data in said shared memory at said particular address of said mapped portion of the shared memory with said consumer computer after receipt of said second signal from said provider computer and extracting said selected data from said shared memory and transferring it into the local memory of said consumer computer; and

transmitting a third signal from said consumer computer to said provider computer that said selected data has been extracted.

The examiner relies on the following reference:

Yamaoka et al. (Yamaoka) 5,214,759 May 25, 1993

Claims 1, 4-8, 12, 13, 16, 17, and 19 stand rejected under 35 U.S.C. § 102 as being anticipated by Yamaoka.

We refer to the Final Rejection (mailed Jan. 31, 1997) and the Examiner's Answer (mailed Feb. 20, 1998) for a statement of the examiner's position and to the Brief (filed Nov. 12, 1997) and the Reply Brief (filed Apr. 24, 1998) for appellants' position with respect to the claims which stand rejected.

OPINION

The Final Rejection sets forth, on pages 2 and 3, the 35 U.S.C. § 102 rejection of independent claims 1, 7, and 13 as being anticipated by Yamaoka. The rejection applies the language of instant claim 13 to the disclosure of Yamaoka, although not in the order of the features set forth in the claim. For example, the rejection refers to "instructing the provider computer to transfer the data to the mapped portion at the address in the shared memory," which paraphrases paragraph "iv" of claim 13. The rejection later refers to "means for facilitating communication to the provider computer that the consumer

computer is ready to extract data from the mapped portion," which paraphrases paragraph "iii" of claim 13.

Appellants, at pages 13 and 14 of the Brief, argue that Yamaoka fails to disclose generation of the claimed first, second and third signals, and further does not teach the "sequence" set forth in the claims. The examiner responds (Answer at 5) that the examiner "does not see any particular sequence mentioned in the claims."

We note that claim 13 is not a process claim. However, as appellants emphasize, the claim does set forth an ordered progression of signals and associated responses, including transmission and reception of a "first signal," a "second signal," and a "third signal." For example, paragraph "iv" sets forth computer readable program code means "for instructing said provider computer after receipt of said first signal to transfer said data to said mapped portion at said address in said shared memory" (emphasis added). Paragraph "iii" sets forth computer readable program means "for transmitting a first signal to said provider computer that said consumer computer is ready to receive and extract data from said shared memory" (emphasis added). Placing the elements of paragraph "iv" before the elements of paragraph "iii" in the statement of the rejection may represent giving no weight to the sequence related to transmission and reception of the "first signal." However, the requirements of the claim cannot be ignored.

In any event, we agree with appellants that the rejection does not show that Yamaoka generates signals as presently claimed. The Final Rejection refers (page 3) to

column 5, lines 53-56 of Yamaoka for disclosure of "a computer readable program code means for facilitating communication to the provider computer that the consumer computer is ready to extract data from the mapped portion." Column 5, lines 53-56 of the reference falls within Yamaoka's "Summary of the Operation," described at column 4, line 28 through column 5, line 63.

The summary provides a general overview of the system shown in Figure 1, which the reference later describes in depth. A send program, by means of the send operating system (OS), requests an allocation of memory in memory 50 within shared memory device 20. Through shared memory device 20, the send OS informs the receive OS of the leading address and size of a communication buffer allocated in memory 50. The send OS sends a communication ID having "1" set in the bit position corresponding to the receive program in the receive OS.

The instructions for sending and receiving a communication ID are distinguished from the instructions from writing/reading data into/from the memory 50. The above-noted section of column 5, lines 53-56 refers to the communication ID temporarily stored in communication ID register 43. If a bit is set for a receive program, hold circuit 40 generates an interrupt request to the corresponding receive subsystem. Upon receiving the interrupt request, the receive OS issues a receive instruction to the shared memory device 20 to read out the value of the communication ID register 43. By this process the receive OS can inform the receive program that data will be transferred via memory 50.

Column 5, lines 53-56 thus describes an interrupt request generated by shared memory device 20 to a receive OS. The interrupt request is shown as element 77 in Figure 7, and described in detail at column 7, lines 13 through 60 of the reference. The interrupt occurs prior to transfer of data in memory 50, depicted in Figure 8. The procedure is thus related to the dynamic allocation of shared memory, prior to the actual message transfer between programs residing in different subsystems.

The rejection thus does not account for, at least, "computer readable program means for transmitting a first signal to said provider computer that said consumer computer is ready to receive and extract data from said shared memory." The identified section of Yamaoka that is deemed to disclose the feature refers to communication from the provider computer to the consumer computer, rather than in the reverse direction. At least paragraph "iv" of claim 13 is also not met by Yamaoka, since there is a requirement of action by the provider computer "after receipt of said first signal."

Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim. Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co., 730 F.2d 1452, 1458, 221 USPQ 481, 485 (Fed. Cir. 1984). While Yamaoka may disclose elements similar to those set forth in instant claim 13, the reference does not disclose the claimed features including the signals that are sent and received between the provider and consumer computer in

implementing data transfer. We therefore do not sustain the rejection of claim 13, nor claims 16, 17, and 19, incorporating the limitations of claim 13.

Each of independent claim 1, drawn to a process, and independent claim 7, drawn to a product, contains language corresponding to that of claim 13 in setting forth ordered sending and receiving of first, second, and third signals between the provider and consumer computers in effecting data transfer between the computers, and particular actions associated with the signals. Since not all the limitations of claim 1, nor all the limitations of claim 7, are met by Yamaoka, we do not sustain the rejection of those claims, nor the remainder of the claims on appeal, 4-6, 8, and 12, depending from claim 1 or 7.

CONCLUSION

The rejection of claims 1, 4-8, 12, 13, 16, 17, and 19 is reversed.

REVERSED

JAMES D. THOMAS Administrative Patent Judge	)))))) BOARD OF PATENT
MICHAEL R. FLEMING Administrative Patent Judge	) APPEALS) AND) INTERFERENCES
HOWARD B. BLANKENSHIP Administrative Patent Judge	))))

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